WHAT IS CLAIMED IS:

1. A multi chip module package structure with low cost and high reliability, comprising:

a substrate;

a plurality of chip package bodies;

a plurality of electrical connect points, electrically connecting the chip package bodies and the substrate;

a plurality of electrical connect pins; and

a package material, enclosing the substrate, connect points, and chip package body.

2. The structure as claimed in claim 1, wherein said chip package body is a chip-scale package (CSP) or wafer level CSP.

3. The structure as claimed in claim 1, wherein at least one of said chip package bodies is a CSP with a wire bonding.

4. The structure as claimed in claim 1, wherein at least one of said chip package bodies is a CSP with a flip chip bonding.

5. The structure as claimed in claim 1, wherein at least one of said chip package bodies is a CSP with a central pad bonding.

6. The structure as claimed in claim 1, wherein said chip package bodies pass burn-in test and function test.

7. The structure as claimed in claim 2, wherein at least one of said chip package bodies is a CSP with a wire bonding.

8. The structure as claimed in claim 2, wherein at least one of said chip

package bodies is a CSP with a flip chip bonding.

9. The structure as claimed in claim 2, wherein at least one of said chip package bodies is a CSP with a central pad bonding.

10. The structure as claimed in claim 2, wherein said chip package bodies pass burn-in test and function test.

11. The structure as claimed in claim 1, wherein said plurality of electrical connect pins are solder balls.

12. The structure as claimed in claim 1, wherein said plurality of electrical connect points are solder balls or gold wires.

13. A multi chip module package structure with low cost and high reliability, comprising:

a substrate;

at least one chip;

one or more than one chip package bodies;

a plurality of electrical connect points, electrically connecting the chip package bodies and the substrate;

a plurality of electrical connect pins; and

a package material, enclosing the substrate, connect points, chips, and chip package bodies.

14. The structure as claimed in claim 13, wherein said chip is a bare chip.

15. The structure as claimed in claim 14, wherein at least one chip is bonded to the substrate by wire bonding or flip chip bonding.

16. The structure as claimed in claim 13, wherein said chip package body

is a chip-scale package (CSP) or wafer level CSP.

17. The structure as claimed in claim 13, wherein at least one of said chip package bodies is a CSP with a wire bonding.

18. The structure as claimed in claim 13, wherein at least one of said chip package bodies is a CSP with a flip chip bonding.

19. The structure as claimed in claim 13, wherein at least one of said chip package bodies is a CSP with a central pad bonding.

20. The structure as claimed in claim 13, wherein said chip package bodies pass burn-in test and function test.

21. The structure as claimed in claim 16, wherein at least one of said chip package bodies is a CSP with a wire bonding.

22. The structure as claimed in claim 16, wherein at least one of said chip package bodies is a CSP with a flip chip bonding.

23. The structure as claimed in claim 16, wherein at least one of said chip package bodies is a CSP with a central pad bonding.

24. The structure as claimed in claim 16, wherein said chip package bodies pass burn-in test and function test.

25. The structure as claimed in claim 13, wherein said plurality of electrical connect pins are solder balls.

26. The structure as claimed in claim 13, wherein said plurality of electrical connect points are solder balls or gold wires.

27. A method of packaging multi chip module at low cost and with high reliability to form multi chip module package containing a plurality of

chips bonded to a substrate as a main body, wherein said method is characterized as: using one or more than one chip package body as CSP, which is electrically connected to the substrate to form said main body.

28. The method as claimed in claim 27, wherein said main body may form a plurality of electrical connect pins and is enclosed by a package material.

29. The method as claimed in claim 28, wherein said plurality of electrical connect pins are solder balls.

30. The method as claimed in claim 27, wherein said chip package body is of chip-scale package (CSP) or wafer level CSP.

31. The method as claimed in claim 27, wherein at least one of said chip package bodies is a CSP with a wire bonding.

32. The method as claimed in claim 27, wherein at least one of said chip package bodies is a CSP with a flip chip bonding.

33. The method as claimed in claim 27, wherein at least one of said chip package bodies is a CSP with a central pad bonding.

34. The method as claimed in claim 27, wherein said chip package bodies pass burn-in test and function test.

35. The method as claimed in claim 30, wherein at least one of said chip package bodies is a CSP with a wire bonding.

36. The method as claimed in claim 30, wherein at least one of said chip package bodies is a CSP with a flip chip bonding.

37. The method as claimed in claim 30, wherein at least one of said chip package bodies is a CSP with a central pad bonding.

38. The method as claimed in claim 30, wherein said chip package bodies pass burn-in test and function test.

39. The method as claimed in claim 27, wherein said chip package body has a height less than 1.00 mm.

40. The method as claimed in claim 27, wherein said chip package body has a plurality of electrical connect points, which are solder balls or gold wires.

add B17